CHIP BURN-IN AND TEST STRUCTURE AND METHOD

ABSTRACT

A burn-in frame having at least one window and including resistors having resistor pads is situated on a flexible layer, and at least one integrated circuit chip having chip pads is situated in the at least one window. Via openings are formed in the flexible layer to extend to the chip pads and the resistor pads. A pattern of electrical conductors is applied over the flexible layer and extending into the vias. The at least one integrated circuit chip is burned in. The burn-in frame may further include fuses, frame contacts, and voltage bias tracks. After burning in the at least one integrated circuit chip, the chip pads can be electrically isolated and the at least one integrated circuit chip can be tested. This method can also be used to burn-in and test multichip modules.